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10/743,619	12/22/2003	Ivan Farkas	200312767-1	7400

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EXAMINER	
MISIURA, BRIAN THOMAS	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,619	FARKAS ET AL.	
	Examiner	Art Unit	
	Brian T. Misiura	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/15/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-6, 14-17, and 19-23 rejected under 35 U.S.C. 102(b) as being anticipated by Chen, U.S. Patent No. 6,507,881.

2. As per claim 1, Chen discloses:
   - A memory comprising a host (column 4 lines 9-12, "host computer makes a request to program the flash ROM", this shows the host computer has instructions stored in a memory) and an image file (column 3 lines 62-65, "firmware code from the host computer **208**", this firmware code must be stored in a memory of the host computer):
   - a processor configured to execute the host (figure 2 numeral 200);
   - an input/output (I/O) controller coupled to the processor (column 3 lines 53-57, figure 2 numerals 204, 200);
   - a management processing system coupled to the I/O controller and comprising a first storage location, a first memory, and a second memory (column 6 lines 11-21, table 2 "DRQ bit", figure 2, numerals 202, 206);
   - the host is configured to cause the processor to store a first portion of the image file in the first memory (column 6 lines 12-14, figure 2), wherein the host is configured to cause the processor to set the first storage location subsequent to storing the first portion in the first memory (column 6 lines 14-17, "DRQ bit", figure 2 and table 2), and wherein the management

processing system is configured to store the first portion of the image file in the second memory in response to detecting that the first storage location has been set (column 6, lines 17-20, figure 2).

3. As per claim 2, Chen discloses a computer system of wherein the management processing system comprises a second storage location (column 6, lines 19-21, "BSY bit", table 2), and wherein the management processing system is configured to set the second storage location subsequent to storing the first portion of the image file in the second memory (column 6, lines 19-21, (sets the BSY bit to 0 to clear it)).

4. As per claim 3, Chen discloses a computer system wherein the management processing system is configured to store information in the first memory prior to setting the second storage location (column 6, lines 11-21 figure 2).

5. As per claim 4, Chen discloses a computer system wherein the information comprises an acknowledge message (column 6 lines 11-21, figure 2).

6. As per claim 5, Chen discloses a computer system wherein the host is configured to cause the processor to store a second portion of the image file in the first memory in response to detecting that the second storage location has been set, wherein the host is configured to cause the processor to set the first storage location subsequent to storing the second portion in the first memory, and wherein the management processing system is configured to store the second portion of the image file in the second memory in response to detecting that the first storage location has been set (The system disclosed in this claim describes the same system of claim 1 but in a second cycle. By stating a second portion of the image file is the same as stating a second image file. Therefore claim 5 is rejected using the same reference material as listed above for claim 1).

7. As per claim 6, Chen discloses a computer system wherein the first storage location comprises a first register, and wherein the second storage location comprises a second register (column 6, lines 11-21, BSY and DRQ register bits, table 2).

8. As per claim 14 Chen discloses a computer system of wherein the processor is configured to cause the portion of image file to be provided to the management processing system using a plurality of messages, and wherein each of the plurality of messages comprises a header and a body (column 6 lines 11-21, figure 2 and table 2, Name of register equivalent to header and bits equivalent to body).

9. As per claim 15, Chen discloses a computer system wherein the image file comprises firmware (column 3 lines 62-65, figure 2).

10. As per claim 16, Chen discloses a computer system wherein the second memory comprises a non-volatile memory (column 6, lines 11-21, figure 2, ROM is a form of non-volatile memory).

11. As per claim 17, Chen discloses: a system comprising: a master (figure 2 numeral 208); a slave (figure 2 numerals 202, 204, 206); a bus coupled to the master and the slave (figure 2 "IDE bus"); a first storage location (column 6 lines 14-17, "DRQ bit", figure 2 and table 2); a second storage location (column 6, lines 19-21, "BSY bit", table 2); and a first memory accessible to the master and the slave (figure 2 numeral 206); wherein the master is configured to store first information in the first memory using the bus (column 6 lines 12-14, figure 2), wherein the master is configured to set the first storage location subsequent to storing the first information using the bus (column 6 lines 14-17, "DRQ bit", figure 2 and table 2), wherein the slave is configured to access the first information in

response to detecting that the first storage location has been set (column 6, lines 17-20, figure 2), wherein the slave is configured to store second information in the first memory subsequent to accessing the first information (column 6, lines 30-42 figure 2), wherein the slave is configured to set the second storage location subsequent to storing the second information (column 6, lines 35-39), and wherein the master is configured to access the second information using the bus in response to detecting that the second storage location has been set (35-42, figure 2).

12. As per claim 19, Chen discloses a system wherein the master comprises a host (column 3 lines 62-65, "firmware code from the host computer **208**").

13. As per claim 20, Chen discloses a system wherein the slave comprises a management processing system (figure 2 numerals 202, 204, 206).

14. As per claim 21, Chen discloses a system wherein the first storage location comprises a first register, and wherein the second storage location comprises a second register (column 6, lines 11-21, BSY and DRQ register bits, table 2).

15. As per claim 22, Chen discloses a system wherein the first information comprises at least a portion of a firmware upgrade (column 3 lines 62-65, figure 2).

16. As per claim 23, Chen discloses a system wherein the second information comprises an acknowledge message (column 6 lines 11-21, figure 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 7-10, 13, 18, 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, U.S. Patent No. 6,507,881, in view of Alexander et al, U.S. Patent No. 6,188,602.

18. As per claim 7, Chen does not disclose a computer system wherein the management processing system comprises a network connection that is configured to provide a remote user with access to the computer system.

However, Alexander discloses a computer system wherein the management processing system comprises a network connection that is configured to provide a remote user with access to the computer system (Alexander, column 3 lines 6-8, figure 1, "local area network (LAN) card" would allow remote user access to the system).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Alexander into the system of Chen to provide remote access to a user via a network connection.

The modification would have been obvious because one having ordinary skill in the art would want to have remote access to the system via a network connection (Alexander, column 3 lines 6-8, figure 1, "local area network (LAN) card" would allow remote user access to the system).

19. As per claim 8, Chen does not disclose a computer system wherein the management processing system is configured to provide status information associated with the computer system to the remote user.

However Alexander discloses a computer system wherein the management processing system is configured to provide status information associated with the computer system to the remote user (column 3 lines 37-49, figure 1).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Alexander into the system of Chen to provide status information to the user of the system in order to help prevent problems from occurring (column 3 lines 37-49, figure 1).

The modification would have been obvious because one having ordinary skill in the art would want to have a way of staying informed on the status of a computer system (column 3 lines 37-49, figure 1).

20. As per claim 9, Chen does not disclose a computer system comprising: a PCI bus coupled to the I/O controller and the management processing system; wherein the I/O controller comprises a PCI controller.

However, Alexander discloses a computer system comprising: a PCI bus (figure 1 numeral 132) coupled to the I/O controller and the management processing system; wherein the I/O controller comprises a PCI controller (column 3 lines 6-8, 25-28, figure 1).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Alexander into the system of Chen to allow for the system to accompany PCI devices.

The modification would have been obvious because one having ordinary skill in the art would want to allow for the system to accompany PCI devices (figure 1 numeral 132) and (column 3 lines 6-8, 25-28, figure 1).

21. As per claim 10, Chen does not disclose a computer system wherein the host is configured to be executed by the processor subsequent to an operating system being booted by the processor.

However, Alexander discloses: a computer system wherein a host is configured to be executed by a processor subsequent to an operating system being booted by the processor (column 4 lines 57-61, figure 1).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Alexander into the system of Chen to allow firmware upgrading while other tasks are running.

The modification would have been obvious because one having ordinary skill in the art would want to allow firmware upgrading while other tasks are running (column 4 lines 57-61, figure 1).

22. As per claim 13, Chen does not disclose a computer system wherein the host is configured to be executed by the processor using an Intermediate System Loader (ISL) protocol.

However, Alexander discloses a computer system wherein the host is configured to be executed by the processor using an Intermediate System Loader (ISL) protocol (column 3 lines 37-49, figure 1).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Alexander into the system of Chen to use such a protocol to allow firmware upgrading while other tasks are running.

The modification would have been obvious because one having ordinary skill in the art would want to use such a protocol to allow firmware upgrading while other tasks are running (column 3 lines 37-49, figure 1).

23. As per claim 18, Chen does not disclose a system wherein the bus comprises a PCI bus.

However, Alexander discloses a system wherein the bus comprises a PCI bus (figure 1 numeral 132).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Alexander into the system of Chen to allow for the system to accompany PCI devices.

The modification would have been obvious because one having ordinary skill in the art would want to allow for the system to accompany PCI devices (figure 1 numeral 132).

24. As per claim 24, Chen discloses, a method performed by a computer system that comprises a management processing system (figure 2 numerals 202, 204, 206) comprising:

- storing first information into a first memory in the management processing system (column 6 lines 12-14, figure 2);

- setting a first storage location in the management processing system to a first value (column 6 lines 14-17, "DRQ bit", figure 2 and table 2);

- accessing the first information in response to detecting that the first storage location has been set to the first value (column 6, lines 17-20, figure 2);

- storing second information into the first memory in response to accessing the first information in the first memory (column 6, lines 30-42 figure 2);

- and setting a second storage location in the management processing system to a second value subsequent to storing the second information (column 6, lines 35-39).

Chen does not disclose the use of an input/output (I/O) bus.

However, Alexander discloses the use of an I/O bus (column 3 lines 6-8, 25-28, figure 1).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Alexander into the system of Chen to have an I/O bus in a computer system with which you can transfer data over.

The modification would have been obvious because one having ordinary skill in the art would want to be able to send data over a bus (column 3 lines 37-49, figure 1).

25. As per claim 25, Chen discloses a method of storing the first information into a second memory in response to accessing the first information (column 6, lines 17-20, figure 2).

26. As per claim 26, Chen discloses a method wherein the first information comprises firmware (column 3 lines 62-65, figure 2), and wherein the second memory comprises a non-volatile memory (column 6, lines 11-21, figure 2, ROM is a form of non-volatile memory).

27. As per claims 27 and 28, the system disclosed in these claims describes the same system of claim 24, but in multiple cycles. By stating multiple versions of the image file is the same as stating a second or third image file. Therefore claims 27 and 28 are rejected using the same reference material as listed above for claim 25).

Chen does not disclose the use of an input/output (I/O) bus.

However, Alexander discloses the use of an I/O bus (column 3 lines 6-8, 25-28, figure 1).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Alexander into the system of Chen to have an I/O bus in a computer system with which you can transfer data over.

The modification would have been obvious because one having ordinary skill in the art would want to be able to send data over a bus (column 3 lines 37-49, figure 1).

29. As per claim 29, Chen discloses a method wherein the first information comprises a start upgrade message, wherein the second information comprises a first acknowledge message, wherein the third information comprises at least a portion of an image file, and wherein the fourth information comprises a second acknowledge message (column 6, lines 11-21 figure 2).

30. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, U.S. Patent No. 6,507,881, in view of Krithivas et al, U.S. Patent No. 6,816,963.

31. As per claim 11, Chen does not disclose a computer system wherein the host is configured to be executed by the processor prior to an operating system being booted by the processor.

However, Krithivas discloses wherein the host is configured to be executed by the processor prior to an operating system being booted by the processor (Krithivas, column 2 lines 60-67, column 3 lines 1-13, figure 5).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Krithivas into the system of Chen to achieve firmware upgrade prior to the operating system being booted.

The modification would have been obvious because one having ordinary skill in the art would want to achieve firmware upgrade prior to the operating system being booted (Krithivas, column 2 lines 60-67, column 3 lines 1-13, figure 5).

32. As per claim 12, Chen does not disclose a computer system wherein the host is configured to be executed by the processor using an Extensible Firmware Interface (EFI) protocol.

However, Krithivas discloses a computer system wherein the host is configured to be executed by the processor using an Extensible Firmware Interface (EFI) protocol (Krithivas, column 2 lines 60-67, column 3 lines 1-13, figure 5).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Krithivas into the system of Chen to achieve firmware upgrade using an EFI interface protocol, prior to the operating system being booted.

The modification would have been obvious because one having ordinary skill in the art would want to achieve firmware upgrade using an EFI interface protocol, prior to the operating system being booted (Krithivas, column 2 lines 60-67, column 3 lines 1-13, figure 5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BTM

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
10/29/05